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HARDWARE DEVELOPMENT. ITEM 0004 OF MICROPROCESSOR-BASED POWER C--ETC(U)
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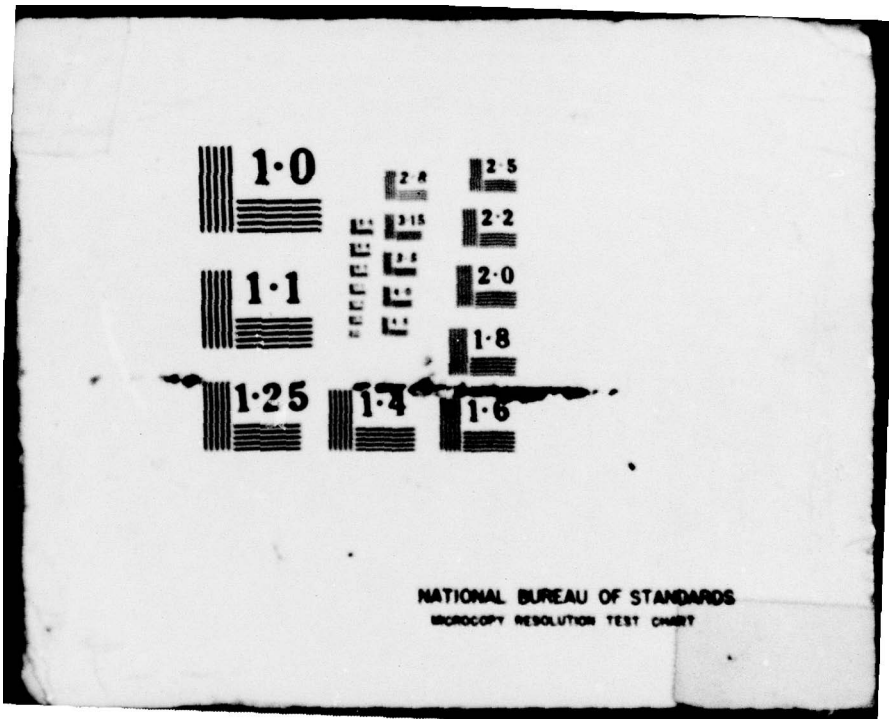
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NATIONAL BUREAU OF STANDARDS
MICROCOPY RESOLUTION TEST CHART

LEVEL II

(6) HARDWARE DEVELOPMENT

ITEM 0004
OF
MICROPROCESSOR-BASED POWER
CONDITIONER CONTROLLER

CONTRACT NO. DAAK70-78-C-0117
(15)

PREPARED FOR
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1.0 SUMMARY

This report covers effort under contract DAAK70-78-C-0117 to develop a microprocessor-based controller for the Delco 15 KW power conditioner.

Continuing from the microprocessor selection, the previous task, the controller hardware was developed and tested during this task. The controller software will be developed in the next task.

The controller hardware conforms closely to the controller baseline design concepts of Task 2. A variation from the baseline did occur in the converter SCR commutation sense circuitry. The existing Delco commutation sense signals will not be used by the controller breadboard. Instead, a more direct and perhaps more reliable method of sensing the converter SCR commutation will be implemented with optical couplers. This method is presented in detail in the report.

Additional hardware, external to the controller, was developed to facilitate testing of the controller breadboard. An interface was developed between the Motorola Exorciser development system and the controller. The Exorciser interface was connected to the empty 6809 microprocessor socket on the controller. Special debug facilities in the Exorciser permitted the microprocessor address, data, and control lines to be exorcised easily from a keyboard. Special circuitry was developed to simulate portions of the power conditioner. The power conditioner simulation devices and the Exorciser development system were used to debug and verify correct operation of the hardware without the 6809 microprocessor and controller software.

2.0.0 PREFACE

The work described in this report was performed by Yucca International, Inc. under the direction of the U. S. Army Mobility Equipment Research and Development Command. This report completes the fourth task of the first phase of the U. S. Army contract no. DAAK-70-78-C-0117. The contracting officer's representative is Dr. David Lee of the U. S. Army MERADCOM Headquarters at Fort Belvoir, Virginia.

3.0.0 COPYRIGHT PERMISSION

No copyright permission is required.

4.0.0 INTRODUCTION

This is a report of the fourth task of six tasks of the U. S. Army contract no. DAAK70-78-C-0117.

Performed during the previous tasks was the baseline design of the controller and selection of an optimum microprocessor. Performed during this task was the development of the controller hardware based on the concepts outlined in Task 2, the baseline design. The objective of this task was to build the necessary hardware to perform voltage and current regulation of the converter section of the Delco 15 KW power conditioner.

The objective also included testing of the hardware to debug any wiring errors and assure that all parts were functional and that the circuitry will work as expected.

Contained in the report is a description of the breadboard and is supplemented with schematics and a parts list.

5.0.0 INVESTIGATION

5.1.0 OVERVIEW

Figure #1 is a block diagram of the controller. The circuitry that will perform the voltage and current regulation function required of the controller during this phase of the contract was breadboarded on two separate wire-wrap boards. The interconnects are made through a motherboard. The microprocessor, EPROM, RAM and input/output are contained on one board and the Converter SCR timing circuitry and sense signal data acquisition circuitry is on the other. An empty slot on the motherboard is reserved for a board which will contain the Inverter SCR timing circuitry and additional circuitry to be developed in the next phase of the contract.

The two boards developed during this phase will be designated as follows:

1) MPU and Peripheral Input/output Board or simply "MPU board;"
2) Sense Signal Aquisition and Converter Timing Board or simply "Board #1."

The circuitry that will be developed during the next phase of the contract will be referred to as Board #2 and it will include the following:

1) Overtemperature sensing circuitry;
2) Slow fan speed sense circuitry;
3) Power supply failure early detection circuitry;
4) Special circuitry used for self-test;
5) Inverter SCR timing circuitry.

Figure #2 shows the general layout of the breadboard and lists the required power supplies.

The controller design uses a combination of TTL, LSTTL, and CMOS. Due to the low power and high noise immunity characteristic of CMOS, it was the preferred family and was used where speed was not critical and if it would not result in a significant increase in package count. If possible and practical, as controller development progresses, more TTL may be replaced by CMOS. The CMOS used on Board #1 is currently deriving its power from the +5 volts supply but may be connected to higher voltages for greater noise immunity and speed of operation if the need arises.

The IC's used in the breadboard, in general, are commercial versions of components that are available in military versions at a higher cost. The parts list, Figure #11, provides the actual component used on the breadboard.

The breadboard conforms very closely to the concepts outlined in the report on task 2, the baseline design of the controller. The only variation occurred in the converter SCR timing circuitry. This variation is due to a change in the way the converter SCR commutation is sensed. The variation will be described in detail later.

For testing purposes, it was necessary to design and build additional hardware external to the controller to simulate the converter SCR's, the front panel controls, and some sense signals. Other additional hardware included circuitry to interface the Motorola Exorciser microcomputer development system to the controller.

The schematics of the additional hardware are included in this report as Figures #14, 15, 16 .

5.2.0 MPU AND PERIPHERAL INPUT/OUTPUT BOARD

This board contains the microprocessor EPROM, RAM, and I/O. It also contains circuitry which generates sync signals used by the sense signal data acquisition circuitry when measuring inverter output voltages. The schematic of the MPU board is shown in Figure #12.

The principal components on the board are two 2716's (for a total of 4K bytes of EPROM), two MC6810's (for 256 bytes of RAM), two MC68B21's.

Sockets are reserved on the board for the MC6809 microprocessor and MC6846 ROM-I/O-timer. They will be implemented when samples become available. The 6846 contains 2K of ROM which can replace one of the 2716's when the software is finalized. The 6846 will also have an 8 bit I/O port that will provide additional I/O capability.

The 8T97's used for buffering the addresses are optional. They can be replaced by 16 pin headers containing jumpers.

A keyboard/display controller has been included on the board to simplify and minimize the components necessary for interfacing to a display. The 8279 will multiplex the displays for less power consumption and allow non-hex characters to be displayed. This feature will be useful for displaying some alpha characters in addition to hexidecimal characters. The 8279 can be connected to an undecoded keyboard which may be used to enter diagnostic or trouble shooting commands when operating the controller free of a development system.

Sufficient board space has been reserved for EPROM and RAM expansion. There are several spare pins available on the motherboard for additional board to board wiring.

The ROM, RAM and I/O addresses assigned to the controller circuitry were chosen to avoid any data bus confliction when using the Exorciser as an MPU for the controller. The MC6809 simulator firmware and debug firmware reside in addresses above D000H in the Exorciser. The controller will be wired to ignore addresses above CFFFH when connected to the Exorciser development system. When the controller is operating stand alone, with its own MPU and software, it must have the capability to respond to addresses between FFFØH and FFFFH. These addresses will contain the MC6809 restart and vector branch table. (Pin 4 and pin 5 of A39 of the MPU board will be connected to ground when the stand alone mode is used.)

Figure #3 is an address map of the controller.

Figure #4 details specific addresses of the hardware.

Figure #5 details how each bit of the data bytes read back from the hardware (enabled by read enable signals) should be interpreted.

The MPU board connects to other parts of the controller and power conditioner via two connectors. P6 is a 50 pin connector which will connect to the power conditioner front panel. The frequency select switch and inverter output voltage BCD thumbwheel switches can be read, and up to 16 7-segment displays can be written over a 50 pin ribbon cable and a mating connector. An unencoded keyboard can be easily connected at a later date to serve as a development aid.

P1 is the 86 pin edge connector on the MPU board.

The controller will initially use the MC6809 and standard speed peripherals. When the hardware is proven and perfected, then faster program execution can be obtained, if desired, by using an MC68B09 microprocessor and faster memory and peripherals.

5.3.0 SENSE SIGNAL ACQUISITION AND CONVERTER TIMING BOARD

Board #1 performs four separate functions. These are:

1) Converter SCR timing signal generation;
2) Monitor converter SCR commutation sense signals;
3) Measure power conditioner sense signals;
4) Count waveform generation sync signals.

The converter SCR timing signals generated on this board will connect to Delco SCR gate drivers in the power conditioner. The frequency of the timing signals are based on a 10 bit digital value programmed into a 10 bit CMOS digital to analog converter.

Board #1 also contains circuitry which will monitor the converter SCR commutation sense signals from the power conditioner.

All of the converter SCR timing signals and SCR commutation signals are routed via P5, a 50 pin connector at the top of the board.

Board #1 contains two A/D converters which are used to measure an analog voltage that is selected by an analog multiplexer. Each A/D converter has a corresponding sample and hold and analog multiplexer associated with it, and is capable of measuring any one of eight channels. Fourteen of the 16 analog channels will connect to 14 sense signals in the power conditioner via P6, a 50 pin connector at the top of the board.

A counter is included on Board #1. It is used to count waveform generation sync pulses between each zero crossing of the Phase A inverter output voltage. The count at any instant can be used to define the number of degrees past zero degrees (or 180^{o}) that ØA is at.

5.3.1 CONVERTER SCR TIMING CIRCUITRY

This circuitry consists of two parts. One part generates a converter oscillator frequency. The other part distributes the pulses coming from the oscillator to six separate outputs. Each output will connect to a pair of converter SCR gate drivers in the power conditioner.

The converter oscillator frequency is generated by a DAC and VCO combination. The Analog Devices AD7522 10 bit CMOS DAC requires an external voltage reference. This is supplied by an AD584JH pin programmable precision voltage reference, that is programmed to +10V, ±30mv.

The AD7522LD used in conjunction with an LM741C operational amplifier will produce a -10 volt output full scale. A binary count of 3FFH loaded into the DAC will correspond to -10 volt output. A count of 000H will correspond to zero volts output.

This analog voltage is used to adjust the current drawn out of pin 6 of the EXAR XR2207C voltage-controlled oscillator. The output frequency of th VCO is adjustable from approximaterly 66Hz to 33KHz in the present configuration. An output frequency of 33KHz will be sufficient to drive to converter SCR's to supply a 15KW load. The procedure for increasing the oscillator frequency to accomodate a load requirement that exceeds 15KW is as follows.

If a DAC count of 3FFH is insufficient to maintain the inverter output voltage at nominal level due to an overload, then change the DAC count from 3FFH to 000H. Program the peripheral line PB5 to go low. This causes pin 9 of the VCO to go high which enable current to flow out of pin 7 of the VCO through R49 and R13. R13 can be adjusted to generate a VCO output frequency equivalent to a DAC count of 3FFH (approximately 33KHz). The output frequency may now be increased from 33KHz (approximate) by increasing the DAC count from 000H. Each time a transition is made from an overload condition to a normal load condition (or vice versa) it would be advisable to follow a procedure similar to the above to prevent possible overshoot or undershoot of inverter output voltage. The total timing current drawn out of pins 6 and 7 of the VCO should never exceed 6MA according to the VCO specification sheet. There are also range limitations on the timing resistors that should be observed if a modification is ever necessary. The optimum power supply for the VCO in this configuration is $\pm$ 6 volts, $\pm$ 7.5 volts is presently used because of convenience, but is well within the operating range of the device. A noteable feature of the VCO is that it has low sensitivity to power supply voltage changes (.15% frequency change per volt; according to the manufacturer specification).

The output of the VCO requires a level conversion to make it compatible with CMOS logic.

The second part of the converter SCR timing circuitry uses pulses coming from the converter oscillator to produce three clocks. Each consecutive oscillator pulse is converted to 12 µs pulse width and then distributed to one of three lines in the following sequence; Phase A clock, Phase B clock, Phase C clock. The frequency of each clock will be 1/3 of the oscillator frequency.

These three clocks are shown leaving Board #1 schematic sheet 1 on the right and entering sheet 3 on the left. Each of the three clocks are delivered to its own corresponding SCR gate logic block. All three gate logic blocks shown on sheet 3 are identical and are associated with the converter SCR commutation sense circuitry. The converter SCR commutation sense signals enter on the left side of sheet 3. The sense signals (12 total) will be low if the corresponding SCR in the converter is conducting and high if it is not. Precautions must be taken to prevent opposite pairs of SCR's in a DC to DC resonant converter from being on at the same time. Therefore, circuitry in this SCR gate logic block examines all four sense signals coming from a DC to DC converter to verify each is high before another SCR pair, or same SCR pair, in that DC to DC converter will be fired. If all four sense signals are high, then the next time a 12 μs clock pulse arrives at the gate logic block, one of the two SCR pair lines (leaving sheet 3 on the right) will go low for 12 μs.

If one of the sense signals had been low when the clock pulse arrived, both of the SCR pair lines would have remained high and an interrupt (comm. fail int., MPU board, sheet 4) would have been issued to the microprocessor. The failing phase is identified by reading peripheral lines PC5, PC6, and PC7. The fail indication will go away automatically if all four SCR's are not conducting when another clock pulse arrives.

The converter SCR timing pulses labeled at the right of Board #1 sheet 3 schematic will alternate automatically between SCR pairs if the SCR pair fired last was verified to have turned on. If both commutation sense signals for an SCR pair do not go low (to indicate that one or both did not turn on) after a firing pulse had been sent to that SCR pair, then the alternate pair of SCR's will not be fired when the next clock

pulse arrives. Therefore, an LED failure in an optical coupler (which is very rare) will cause the opposite pair of SCR's not to receive any firing pulses. The controller will recognize a fail condition has occurred because the power output of the failing converter will drop below that of the other two converters.

The 12 converter commutation sense signals will be generated in the power conditioner from open collector outputs of 12 optical couplers. These 12 lines will be pulled high through pull-up resistors to the CMOS power supply level.

The optical coupler should be mounted close to the converter SCR's in the power conditioner to keep high voltage way from the controller boards. Figure #6 shows how the LED in the optical couplers will be connected to a resonant converter.

6.0.0 DISCUSSION

The circuitry that will be used to perform voltage and current regulation of the converter section of the Delco 15 KW power conditioner was built. Also developed, was the circuitry that will measure inverter output voltage and current. This circuitry was developed during this phase instead of the next phase, for convenience. The circuitry necessary to correlate inverter output voltage measurements to an exact point on the output sine wave was also developed and exists on the breadboard except for the Phase A zero crossing detector which will be designed later.

Not developed during this task was the sense signal conditioning circuitry that will attenuate and filter the signals to a level suitable for measurement by the controller. The sense signals measured by A/D #1 must be in the range of -5v to +5v. A/D #2 will measure voltages between 0v and +10v. An optimum amount of filtering will be required

to remove unwanted ripple or noise but not slow or delay sense signal response. The sense signal conditioning circuitry will be developed after the sense signal outputs have been characterized and specific information about the sense signal waveforms is known.

The sense signal data acquisition circuitry on the controller breadboard was tested by measuring adjustable voltage sources. Voltages between 0 and +5v, in .5 volt increments were presented to the analog multiplexer inputs. The typical accuracy of the digital output of the A/D converters was .1% error, well below .25% error which would be suitable for controlling the inverter output voltage to within 1%.

The converter SCR commutation sense signal circuitry on the controller was developed to monitor the outputs of 12 optical couplers, instead of the existing Delco converter SCR commutation sense signals. This variation from the baseline design is expected to increase the reliability of the power conditioner while removing the need for one transformer (T2) and other components.

The 12 optical couplers, if implemented in the final power conditioner design, will replace the following components which are shown on page 6-4 and page 6-10 of Final Report AC-DC section, contract no. DAAK70-77-C-0035.

T2A, T2B, T2C, CR7-CR18, R7-R9	p. 6-4
R1-R6, R7-R30, C1-C12, U1, 1/2 U2	p. 6-10

The optical sensing method would require the following parts to be added to the power conditioner converter:

12 optical couplers

12 series resistors

12 protection diodes

12 pull-up resistors.

The optical couplers will sense each SCR directly. The present sensing circuitry will sense pairs of SCR's indirectly. Refer to the report of Task 1, of this contract, section 5.1.2 for a description of the Delco sensing method. The optical coupler sense circuitry will be tested with the Delco 15 KW power conditioner when the power conditioner is available.

7.0.0 CONCLUSIONS

The hardware has been designed, constructed, and tested to the level practical before the software has been written. It is expected that some minor changes to the hardware may be necessary as software is being written and debugged.

8.0.0 RECOMMENDATIONS

It is recommended that Yucca International proceed immediately to the next task, development of the controller software.

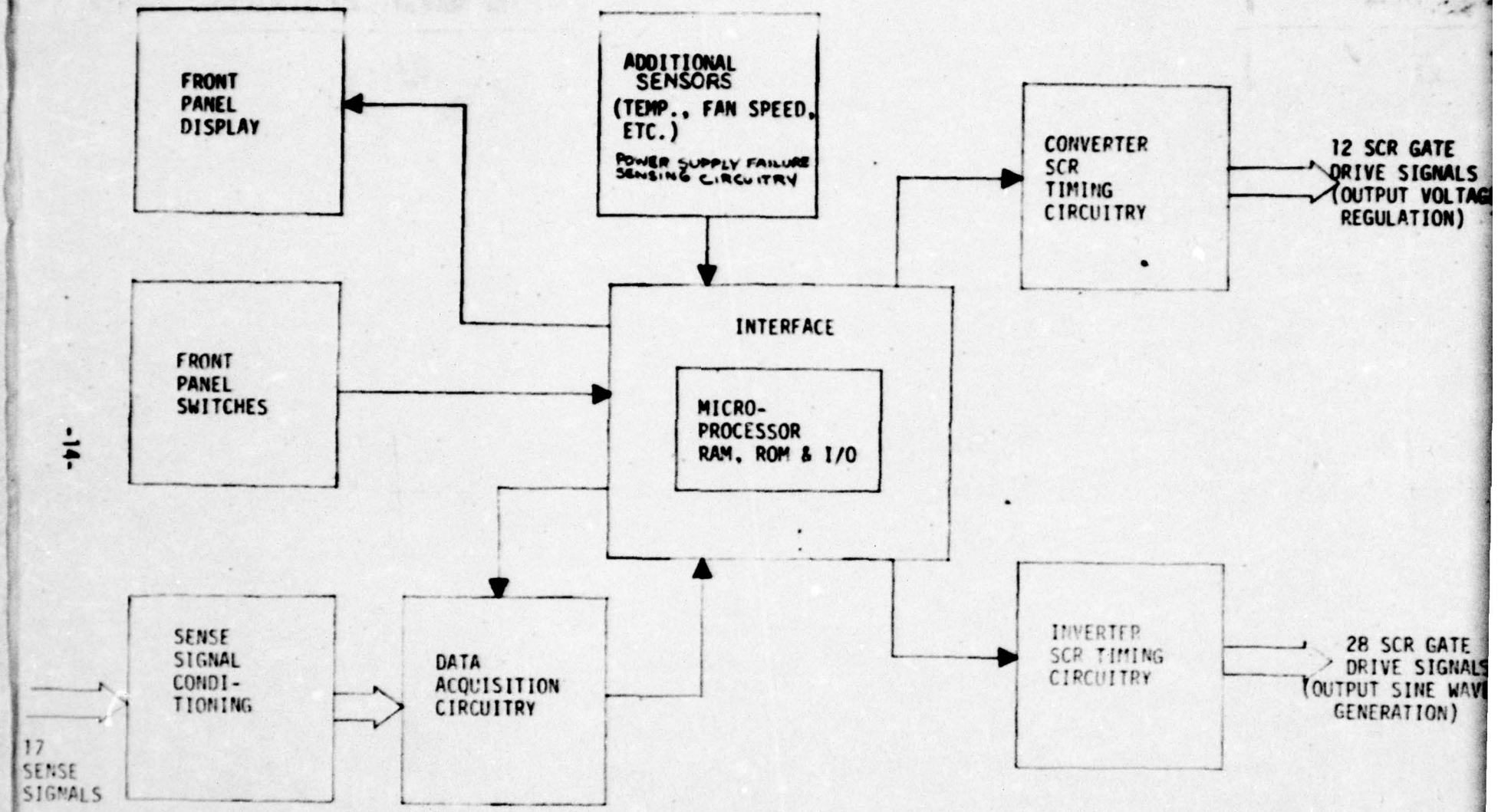
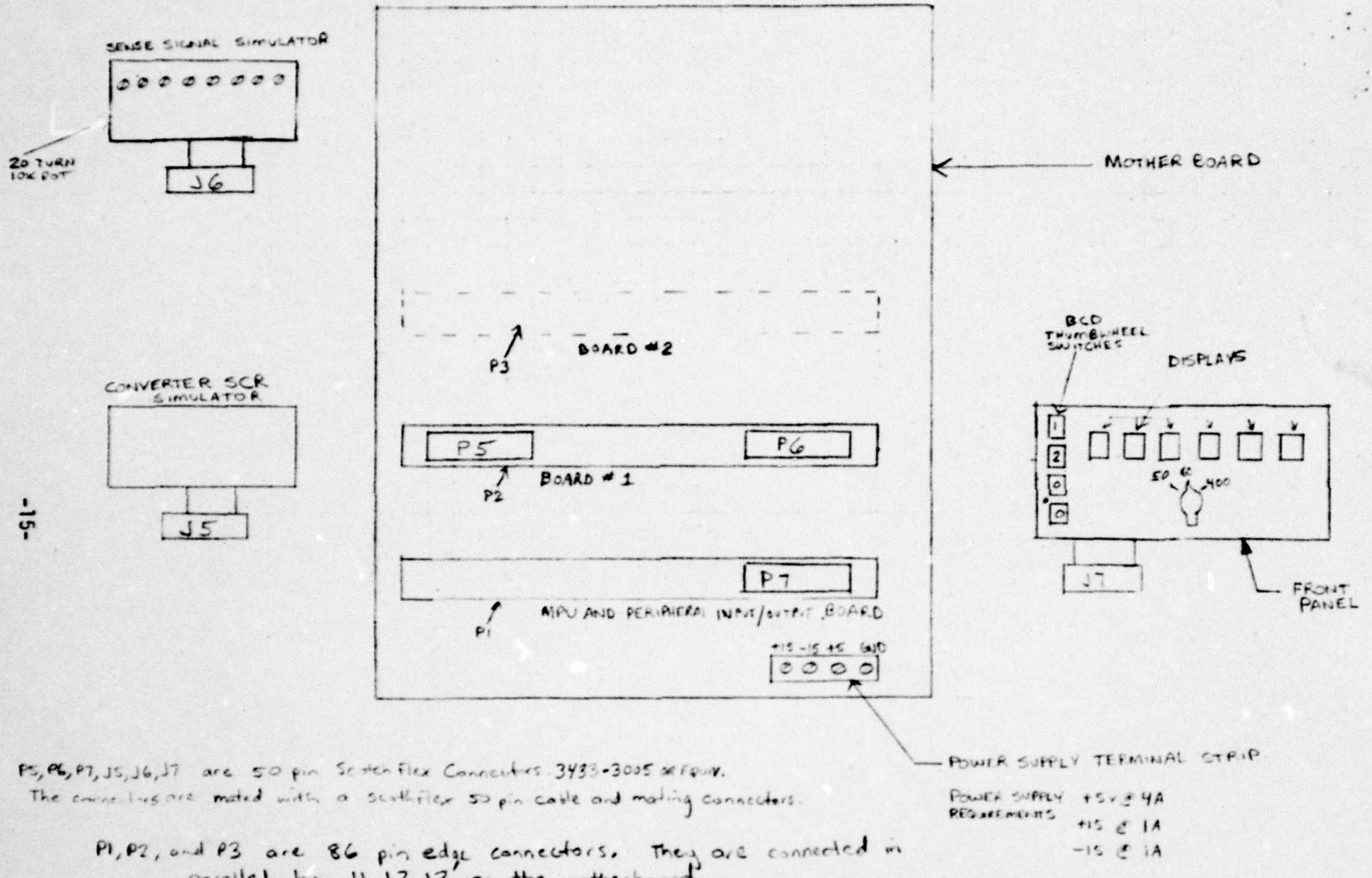


FIGURE 1: CONTROLLER FUNCTIONAL BLOCKS



P5, P6, P7, J5, J6, J7 are 50 pin Scotchflex Connectors 3433-3005 or equiv.
The connectors are mated with a Scotchflex 50 pin cable and mating connectors.

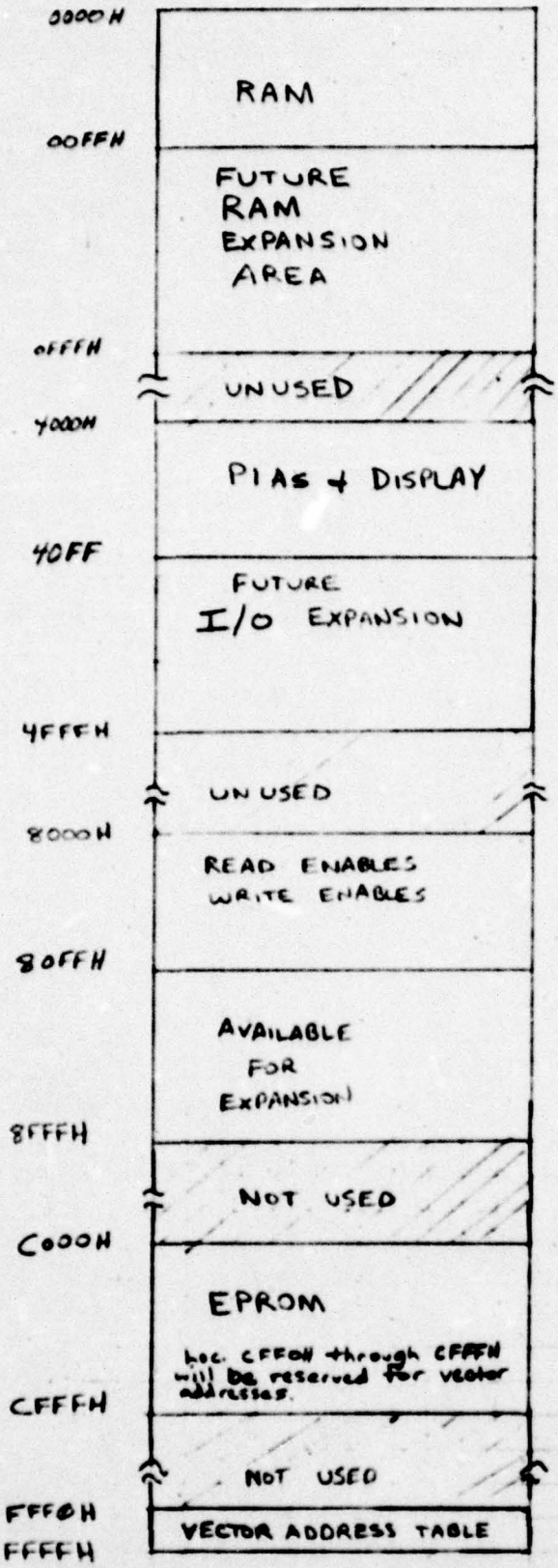
P1, P2, and P3 are 86 pin edge connectors. They are connected in parallel by J1, J2, J3 on the motherboard.

POWER SUPPLY REQUIREMENTS
+5 V @ 4A
+15 @ 1A
-15 @ 1A

CONTROLLER BREADBOARD PHYSICAL CONFIGURATION
FIGURE 2

ADDRESS MAP

ADDRESS MAP
FIGURE 3



Note: The controller will respond to addresses between FFF0H and FFFFH only when it is being operated free of the Exorciser Development System. The vector address table is actually at loc. CFF0H - CFFFH.

0000H - 00FFH RAM

4000H	DISPLAY DATA BUFFER
4001H	DISPLAY COMMAND BUFFER

40A0	PERIPHERAL REGISTER A OR DATA DIRECTION REGISTER A
40A1	CONTROL REGISTER A
40A2	PERIPHERAL REGISTER B OR DATA DIRECTION REGISTER B
40A3	CONTROL REGISTER B

40C0	PERIPHERAL REGISTER C OR DATA DIRECTION REGISTER C
40C1	CONTROL REGISTER C
40C2	PERIPHERAL REGISTER D OR DATA DIRECTION REGISTER D
40C3	CONTROL REGISTER D

WRITE ENABLE SIGNALS

8000	$\overline{WE0}$	DIGITAL TO ANALOG CONVERTER LO BYTE
8001	$\overline{WE1}$	DIGITAL TO ANALOG CONVERTER HI BYTE
8002	$\overline{WE2}$	SPARE
8003	$\overline{WE3}$	SPARE
8004	$\overline{WE4}$	LOAD DAC
8005	$\overline{WE5}$	CLEAR COMMUTATION FAIL INTERRUPT
8006	$\overline{WE6}$	SPARE
8007	$\overline{WE7}$	SPARE

READ ENABLE SIGNALS

8000	$\overline{RE0}$	SPARE
8008	$\overline{RE1}$	A/D #2 BYTE
8010	$\overline{RE2}$	A/D #1 LO BYTE
8018	$\overline{RE3}$	A/D #1 HI BYTE
8020	$\overline{RE4}$	1/4° COUNTER LO BYTE
8028	$\overline{RE5}$	1/4° COUNTER HI BYTE
8030	$\overline{RE6}$	BCD SWITCH LO BYTE
8038	$\overline{RE7}$	BCD SWITCH HI BYTE
8040	$\overline{RE8}$	FREQUENCY SWITCH
8048	$\overline{RE9}$	WAVEFORM EPROM
8050	$\overline{RE10}$	SPARE
8058	$\overline{RE11}$	SPARE
8060	$\overline{RE12}$	SPARE
8068	$\overline{RE13}$	SPARE
8070	$\overline{RE14}$	SPARE
8078	$\overline{RE15}$	SPARE

ADDRESS ASSIGNMENT

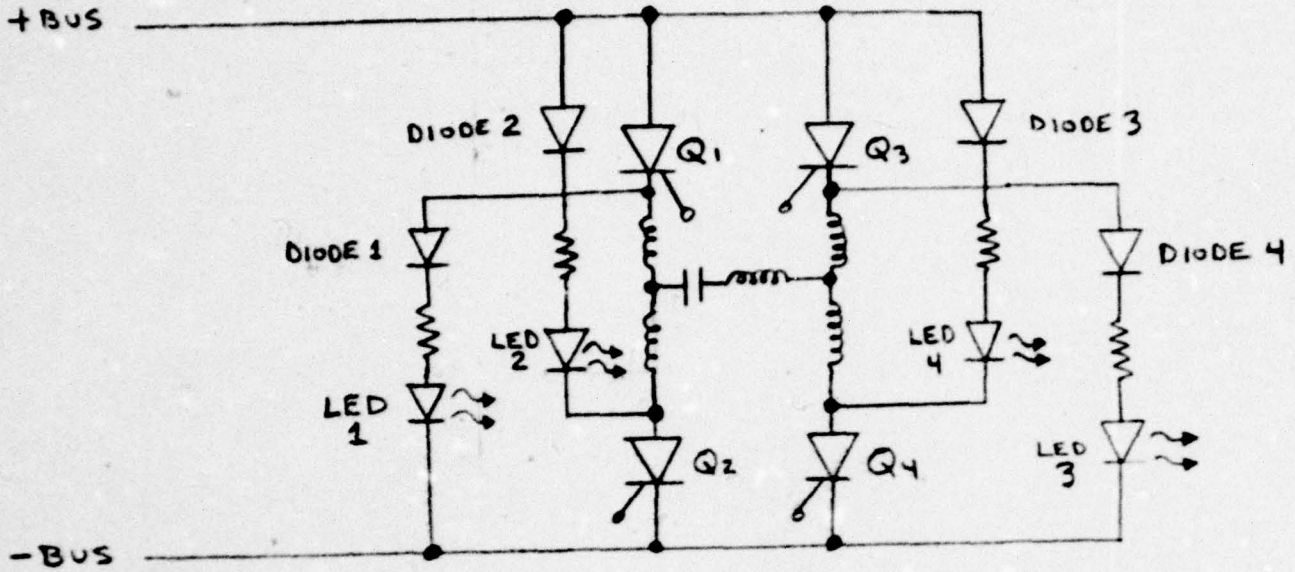
C000H - CFFFH EPROM

FIGURE 4

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
					400HZ	60HZ	50HZ	RE8 (READ FREQUENCY SWITCH)
X	X	X	X	X	0	1	1	RE8 400HZ Selected
X	X	X	X	X	1	0	1	RE8 60HZ Selected
X	X	X	X	X	1	1	0	RE8 50HZ Selected
MOST SIGNIFICANT BCD DIGIT				2ND MOST SIGNIFICANT BCD DIGIT				
8	4	2	1	8	4	2	1	RE7 (READ BCD THUMBWHEEL SWITCHES)
3RD MOST SIGNIFICANT BCD DIGIT				LEAST SIGNIFICANT BCD DIGIT				
8	4	2	1	8	4	2	1	RE6 (READ BCD THUMBWHEEL SWITCHES)
1/4° COUNTER UPPER BYTE								
B15	B14	B13	B12	B11	B10	B9	B8	RE5 (READ 1/4° COUNTER HI BYTE)
1/4° COUNTER LOWER BYTE								
B7	B6	B5	B4	B3	B2	B1	B0	RE4 (READ 1/4 COUNTER LO BYTE)
A/D#1 HI BYTE								
B9	B8	B7	B6	B5	B4	B3	B2	RE3 (READ A/D#1 HI BYTE)
A/D#1 LO BYTE								
X	X	X	X	X	X	B1	B0	RE2 (READ A/D#1 LO BYTE)
A/D#2 BYTE								
B7	B6	B5	B4	B3	B2	B1	B0	RE1 (READ A/D#2 BYTE)

BIT INTERPRETATION OF DATA READ FROM HARDWARE

FIGURE 5



Notes:
1. LED is part of optical coupler. A suitable optical coupler may be a Hewlett Packard HCPL-2601 (5082-4361)
2. LED 1 senses Q1, LED2 senses Q2, ect.
3. DIODES 1-4 are protection diodes.

SIMPLIFIED DIAGRAM OF RESONANT CONVERTER WITH OPTICAL COUPLER SENSING.

FIGURE 6

P5 PIN LIST

PIN				
1	ØA	Q3	OFF	SENSE
2	ØA	Q2	"	"
3	ØA	Q4	"	"
4	ØA	Q1	"	"
5	ØB	Q3	OFF	SENSE
6	ØB	Q2	"	"
7	ØB	Q4	"	"
8	ØB	Q1	"	"
9	ØC	Q3	OFF	SENSE
10	ØC	Q2	"	"
11	ØC	Q4	"	"
12	ØC	Q1	"	"

CONVERTER SCR COMMUTATION SENSE SIGNALS

LOW = SCR ON
HIGH = SCR OFF

13	VCMOS
14	+5V
15	
16	
17	
18	GND

44	DISABLE CONVERTER
45	$\overline{Q3A}$, $\overline{Q2A}$
46	$\overline{Q4A}$, $\overline{Q1A}$
47	$\overline{Q3B}$, $\overline{Q2B}$
48	$\overline{Q4B}$, $\overline{Q1B}$
49	$\overline{Q3C}$, $\overline{Q2C}$
50	$\overline{Q4C}$, $\overline{Q1C}$

CONVERTER SCR FIRING PULSES

CONNECTOR P5 PIN LIST

FIGURE 7

PIN LIST

P6

PIN	SENSE SIGNAL	
1	SPARE CHANNEL	LO
2	" "	HI
3	INVERTER INPUT CURRENT	LO
4	" " "	HI
5	ØA INVERTER OUTPUT VOLTAGE	LO
6	" " " "	HI
7	ØB INVERTER OUTPUT VOLTAGE	LO
8	" " " "	HI
9	ØC INVERTER OUTPUT VOLTAGE	LO
10	" " " "	HI
11	ØA INVERTER OUTPUT CURRENT	LO
12	" " " "	HI
13	ØB INVERTER OUTPUT CURRENT	LO
14	" " " "	HI
15	ØC INVERTER OUTPUT CURRENT	LO
16	" " " "	HI
17	SPARE CHANNEL	LO
18	" "	HI
19	CONVERTER OUTPUT VOLTAGE	LO
20	" " "	HI
21	ØA INPUT VOLTAGE	LO
22	" " "	HI
23	ØB INPUT VOLTAGE	LO
24	" " "	HI
25	ØC INPUT VOLTAGE	LO
26	" " "	HI
27	ØA CONVERTER OUTPUT VOLTAGE	LO
28	" " " "	HI
29	ØB CONV. OUT. VOLTAGE	LO
30	" " " "	HI
31	ØC CONV. OUT VOLTAGE	LO
32	" " "	HI
33		
34	+5V	
35		
36		
37		
38	GROUND	

CONNECTOR PG PIN LIST
FIGURE 8

P7 PIN LIST

PIN	
1	SCAN LINE 0
2	SCAN LINE 1
3	SCAN LINE 2
4	SCAN LINE 3
5	SEGMENT A
6	" B
7	" C
8	" D
9	" E
10	" F
11	" G
12	" DP
13	
14	BLANK
15	DB0
16	DB1
17	DB2
18	DB3
19	DB4
20	DB5
21	DB6
22	DB7
23	BCD SWITCH LOWER BYTE READ ENABLE ($\overline{RE6}$)
24	BCD SWITCH UPPER BYTE READ ENABLE ($\overline{RE7}$)
25	FREQUENCY SWITCH READ ENABLE ($\overline{RE8}$)
26	+5v
27	
28	
29	
30	GND
31	
32	
33	RETURN LINE 0
34	RETURN LINE 1
35	RETURN LINE 2
36	RETURN LINE 3
37	RETURN LINE 4
38	RETURN LINE 5
39	RETURN LINE 6
40	RETURN LINE 7

CONNECTOR P7 PIN LIST

FIGURE 9

PIN #		
A	+5V	
B	+5V	
C	+5V	
D	VCMOS	
E	+15V	
F	+15V	
H		
J	-15V	
K	$\overline{RE0}$	SPARE
L	$\overline{RE1}$	A/D # 2 BYTE READ ENABLE
M	$\overline{RE2}$	A/D # 1 LO BYTE READ ENABLE
N	$\overline{RE3}$	A/D # 1 HI BYTE READ ENABLE
P	$\overline{RE4}$	1/4° COUNTER LO BYTE READ ENABLE
R	$\overline{RE5}$	1/4° COUNTER HI BYTE READ ENABLE
S	$\overline{RE9}$	WAVEFORM EPROM READ ENABLE
T		
U	$\overline{FIRQ}$	
V	$\overline{RESET}$	
W	$\overline{IRQ}$	
X		
Y	GND	
Z	GND	
A	1/4°	
B	10°	
C		
D		
E		
F		
H		
J		
K		
L		
M	PC0	$\overline{CONVERT\ 1}$
N	PC1	10°/$\overline{NORMAL\ MODE}$
P	PC2	SPARE
R	PC3	$\overline{COMPLETE\ 1}$
S	PC4	$\overline{COMPLETE\ 2}$
T	PC5	$\overline{\emptyset C\ FAIL}$
U	PC6	$\overline{\emptyset B\ FAIL}$
V	PC7	$\overline{\emptyset A\ FAIL}$
X	GND	
Y	GND	
Z	GND	

EDGE CONNECTOR P1, P2, P3 PIN LIST

FIGURE 10
PART 1 OF 2

PIN #		
1	+5v	
2	+5v	
3	+5v	
4	VCMOS	
5	+15	
6	+15	
7	-15	
8	$\overline{\text{NMI}}$	
9	DB0	
10	DB1	
11	DB2	
12	DB3	
13	DB4	
14	DB5	
15	DB6	
16	DB7	
17	$\overline{\text{WE0}}$	DIGITAL TO ANALOG CONVERTER LO BYTE WRITE ENABLE
18	$\overline{\text{WE1}}$	DIGITAL TO ANALOG CONVERTER HI BYTE WRITE ENABLE
19	$\overline{\text{WE2}}$	SPARE
20	$\overline{\text{WE3}}$	SPARE
21	GND	
22	GND	
23	$\overline{\text{WE4}}$	LOAD DAC
24	$\overline{\text{WE5}}$	CLEAR COMMUTATION FAIL INTERRUPT
25	PA0	} WAVEFORM GENERATION EPROM READ SELECT
26	PA1	
27	PA2	} MUX # 1 SELECT
28	PA3	
29	PA4	
30	PA5	} MUX # 2 SELECT
31	PA6	
32	PA7	
33	PB0	} OUTPUT FREQ SELECT
34	PB1	
35	PB2	DISABLE PHASE A CONVERTER
36	PB3	DISABLE PHASE B CONVERTER
37	PB4	DISABLE PHASE C CONVERTER
38	PB5	CONVERTER OSCILLATOR 33KHZ OFFSET
39	PB6	DISABLE CONVERTER
40	PB7	$\overline{\text{CONVERT 2}}$
41	GND	
42	GND	
43	GND	

EDGE CONNECTOR P1, P2, P3 PIN LIST

FIGURE 10

PART 2 OF 2

FIGURE 11
PARTS LIST

A 1	CD4097 BE	
A 2	AD 582 KD	ANALOG DEVICES
A 3	AD 571 JD	ANALOG DEVICES
A 4	7474N	
A 5	7406 N	
A 6	7407 N	
A 7	74LS 32	
A 8	8T 97	
A 9	8T 97	
A 10	8T 97	
A 11	AD571 JD	ANALOG DEVICES
A 12	AD 582 KD	ANALOG DEVICES
A 13	CD 4097 BE	
A 14	74 LS 374	
A 15	74 LS 374	
A 16	74 LS 393	
A 17	74LS 393	
A 18	CD 4017 BE	
A 19	CD 4050 BE	
A 20	CD 4098 BE	
A 21	CD 4073 BE	
A 22	AD 584 JH	
A 23	7402	
A 24	LM 741 C	
A 25	AD 7522LD	ANALOG DEVICES
A 26	XR 2207C	EXAR
A 27	MC 6809	(NOT AVAILABLE) MOTOROLA
A 28	2716	INTEL
A 29	2716	INTEL
A 30	MC 6810	MOTOROLA
A 31	MC 6810	MOTOROLA
A 32	MC 68B21	MOTOROLA
A 33	MC 68B21	MOTOROLA
A 34	MC 6846	(NOT AVAILABLE) MOTOROLA
A 35	8216	INTEL
A 36	8216	INTEL
A 37	74LS138	
A 38	74LS154	
A 39	74LS138	
A 40	8T 97	
A 41	8T 97	
A 42	8T 97	
A 43	74LS32	
A 44	74LS04	
A 45	8279	INTEL

CONTROLLER PARTS LIST

FIGURE 11
Part 1 of 4

A	46	CD 4050 BE
A	47	CD 4071 BE
A	48	CD 4071 BE
A	49	CD 4071 BE
A	50	CD 4013 BE
A	51	CD 4013 BE
A	52	CD 4013 BE
A	53	CD 4011 BE
A	54	CD 4011 BE
A	55	CD 4011 BE
A	56	CD 4082 BE
A	57	CD 4082 BE
A	58	CD 4081 BE
A	59	7406
A	60	74LS 11
A	61	74LS04
A	62	CD 4093 BE
A	63	CD 4001 BE
A	64	CD 4018 BE
A	65	CD 4018 BE
A	66	CD 4018 BE
A	67	CD 4018 BE
A	68	74LS 352
A	69	CD 4011 BE
A	70	CD 4013 BE
A	71	CD 4018 BE
A	72	CD 4081 BE

Q1	2N2222
Q2	2N 2222
Q3	2N 2222
Q4	2N 2907

CONTROLLER PARTS LIST

FIGURE 11
Part 2 of 4

R1	4.7K, 10%, 1/4 watt
R2	4.7K, 10%, 1/4 watt
R3	4.7K, 10%, 1/4 watt
R4	15Ω, 5%, 1/4 watt
R5	2.7Ω, 5%, 1/4 watt
R6	2.7Ω, 5%, 1/4 watt
R7	15Ω, 5%, 1/4 watt
R8	10K POT
R9	5.1K, 10%, 1/4 watt
R10	4.7K, 10%, 1/4 watt
R11	1 MEG. 5%, 1/4 watt
R12	500Ω POT
R13	10K POT
R14	500Ω POT
R15	1KΩ, 10%, 1/4 watt
R16	6K, 10% 1/4 watt
R17	12K, 10%, 1/4 watt
R18	560K, 10%, 1/4 watt
R19	4.7K, 10%, 1/4 watt
R20	5.1K, 10%, 1/4 watt
R21	5.1K, 10%, 1/4 watt
R22	5.1K, 10%, 1/4 watt
R23	4.7K, 5%, 1/4 watt
R24	5.1K, 10%, 1/4 watt
R25	4.7K, 10%, 1/4 watt
R26	4.7K, 10%, 1/4 watt
R27	4.7K, 10%, 1/4 watt
R28	10K, 10%, 1/4 watt
R29	10K, 10%, 1/4 watt
R30	10K, 10%, 1/4 watt
R31	10K POT
R32	10K, 10% 1/4 watt
R33	10K, 10%, 1/4 watt
R34	10K, 10%, 1/4 watt
R35	680Ω, 10%, 1/4 watt
R36	680Ω, 10%, 1/4 watt
R37	680Ω, 10%, 1/4 watt
R38	3KΩ, 10%, 1/4 watt
R39	3KΩ, 10%, 1/4 watt
R40	3KΩ, 10%, 1/4 watt
R41	NOT USED
R42	150Ω, 10%, 1/2 watt
R43	150Ω, 10%, 1/2 watt
R44	4.7K, 10%, 1/4 watt
R45	20 MEG, 10% 1/4 watt
R46	22K, 10%, 1/4 watt
R47	10K POT
R48	2.7K, 10%, 1/4 watt
R49	2.2K, 10% 1/4 watt
RPBO-7	10K, 10%, 1/4 watt

CONTROLLER PARTS LIST

FIGURE 11
Part 3 of 4

CR1	DIODE, SILICON, IN914	
CR2	DIODE, SHOTTKY, IN5821	
CR3	DIODE, SILICON, IN914	
CR4	DIODE, ZENER, IN4101,	8.2v
CR5	DIODE, ZENER, IN4101,	8.2v
CR6	DIODE, ZENER, IN4101,	8.2v
CR7	DIODE, SHOTTKY, IN5821	
CR8	NOT USED	
CR9	DIODE, ZENER, IN4737,	7.5v
CR10	DIODE, ZENER, IN4737,	7.5v

SW1 SWITCH, MOMENTARY CONTACT, NORM. CLOSED, PUSHBUTTON

C1, C3	300 pF
C2, C4	1 uF, 35v
C5	.002 uF
C6	.012 uF
C7, C8, C9, C10, C17, C18	.1 uF
C11, C12, C13	1 uF
C14	20pf
C15	26 pf
C16	470 pf

XTAL 1	4.00 MHz
XTAL 2	1.728 MHz

CONNECTOR, EDGE 43/86 PIN SOLDER TAIL, STANFORD APPLIED ENGINEERING SAC-43D/2-2

CONNECTOR, WIRE-WRAP, RIGHT ANGLE . 50 PIN TYB ANGSLEY 609-50X2M
MOTOROLA WIRE-WRAP MODULE MOTOROLA MEX 68 WW

CONTROLLER PARTS LIST
FIGURE 11
Part 4 of 4

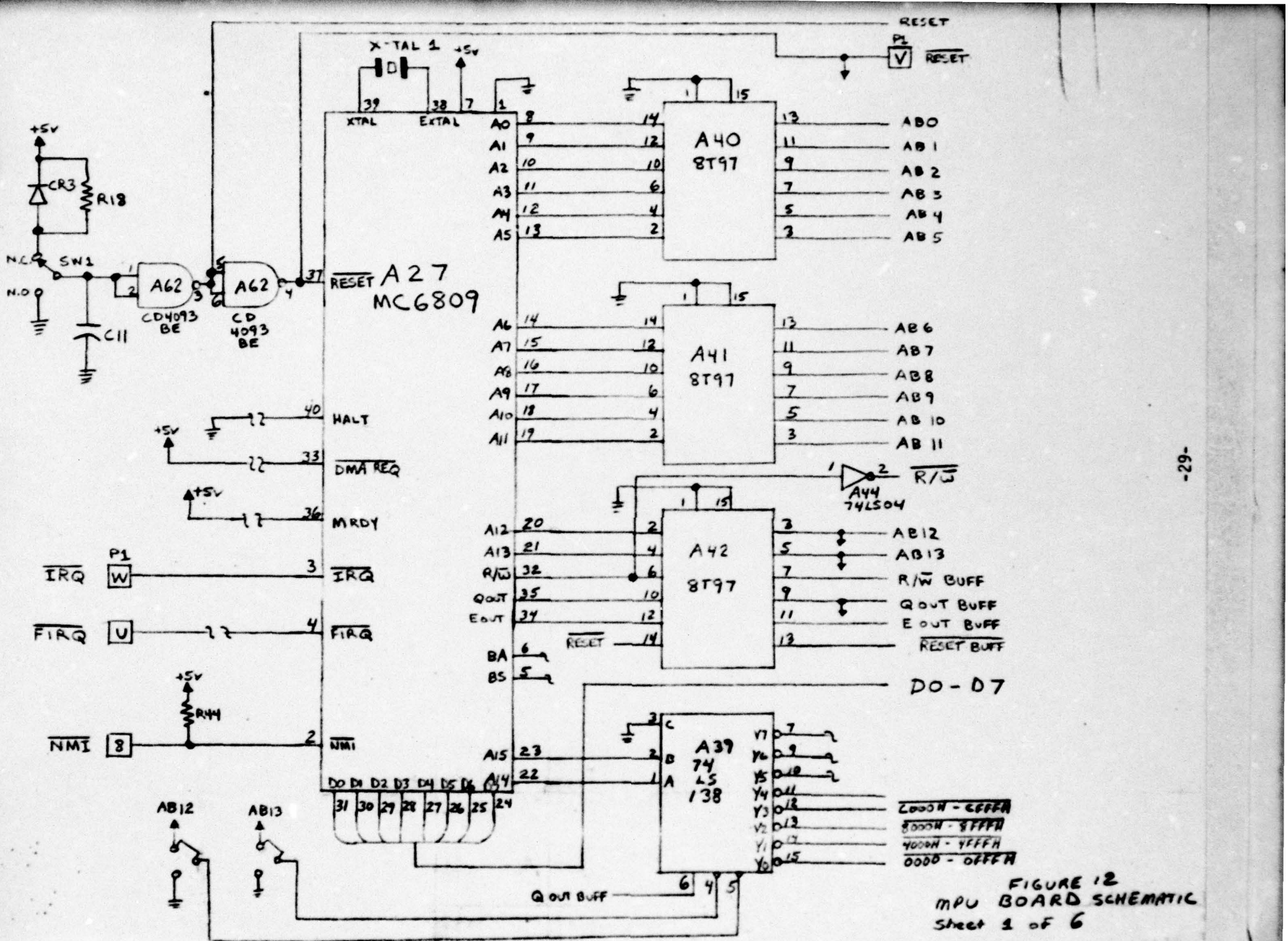
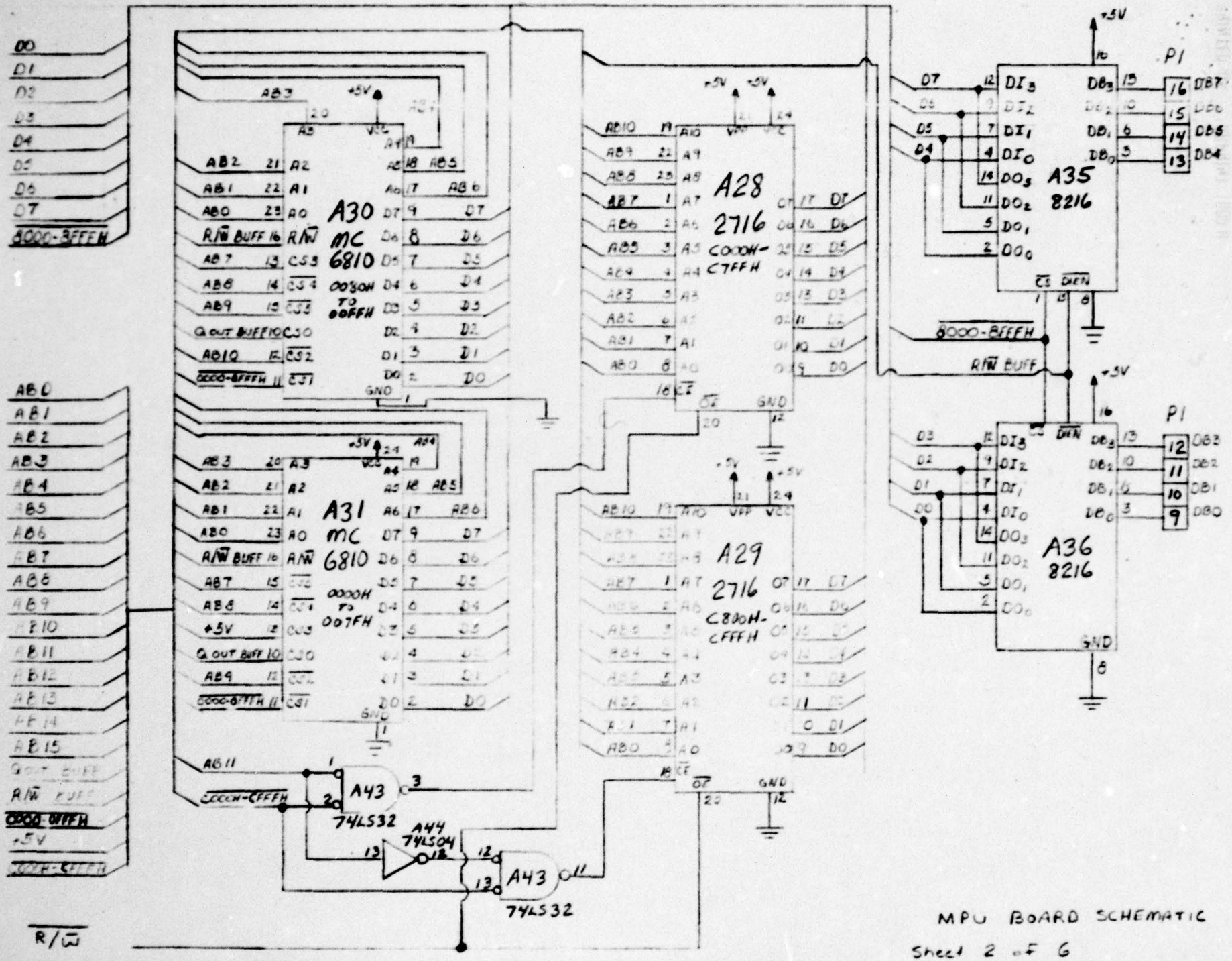
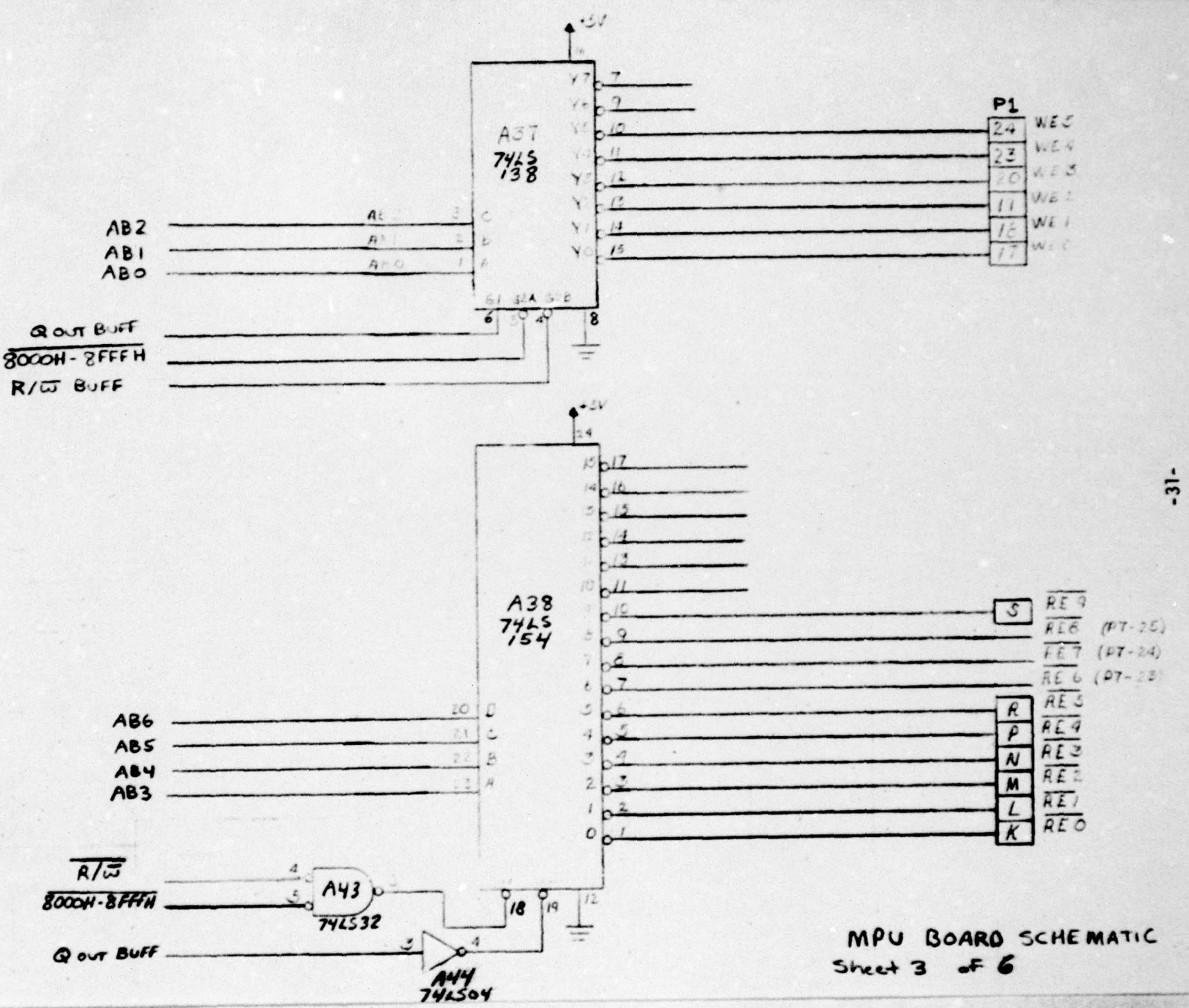
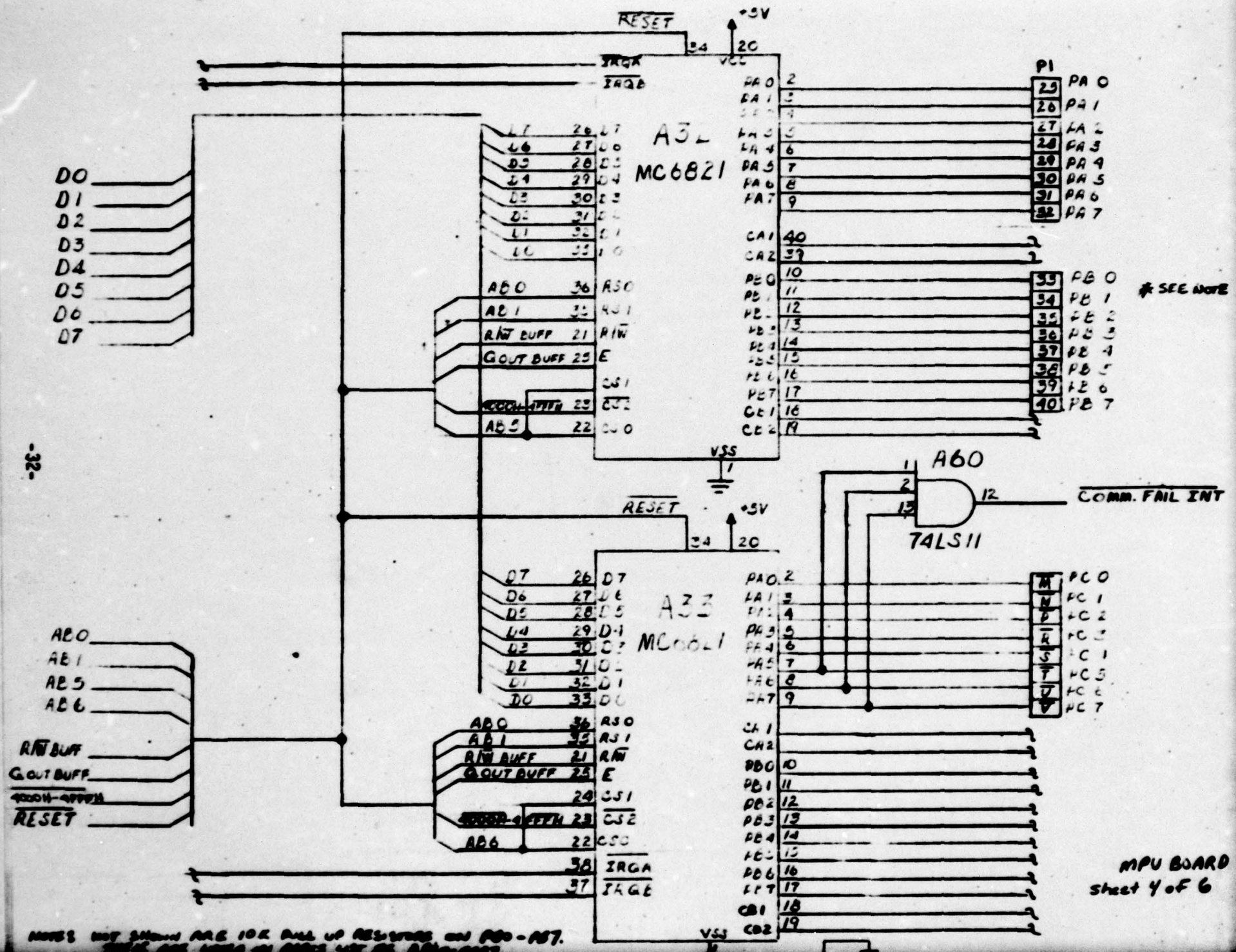


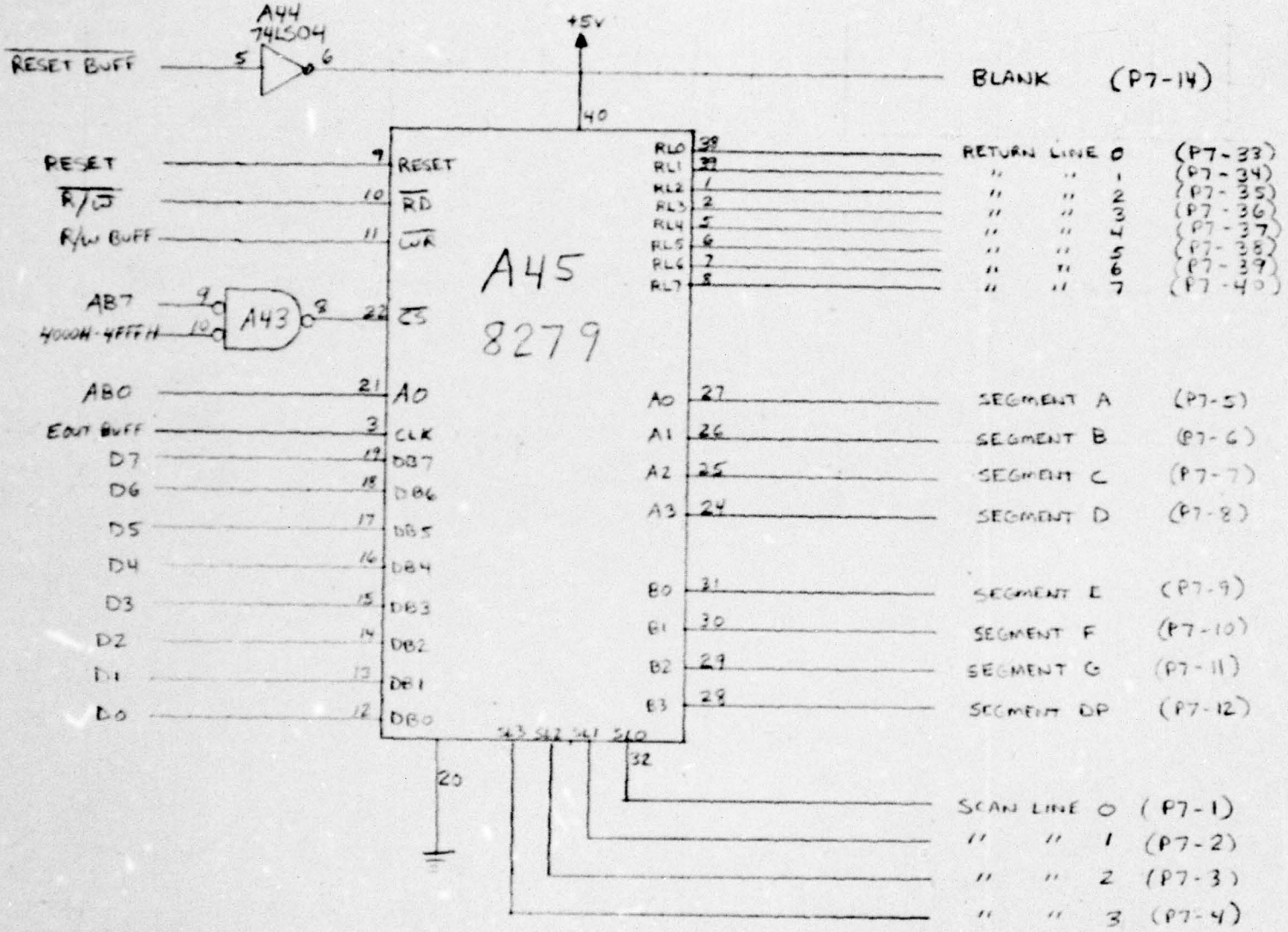
FIGURE 12
MPU BOARD SCHEMATIC
Sheet 1 of 6


A30 MC 6810 0080H TO 00FFH
A31 MC 6810 0000H TO 007FH
A28 2716 C000H-C7FFH
A29 2716 C800H-CFFFH
A35 8216
A36 8216
A43 74LS32
A44 74LS04
A43 74LS32
P1
P1
+5V
GND
R/W
MPU BOARD SCHEMATIC
Sheet 2 of 6

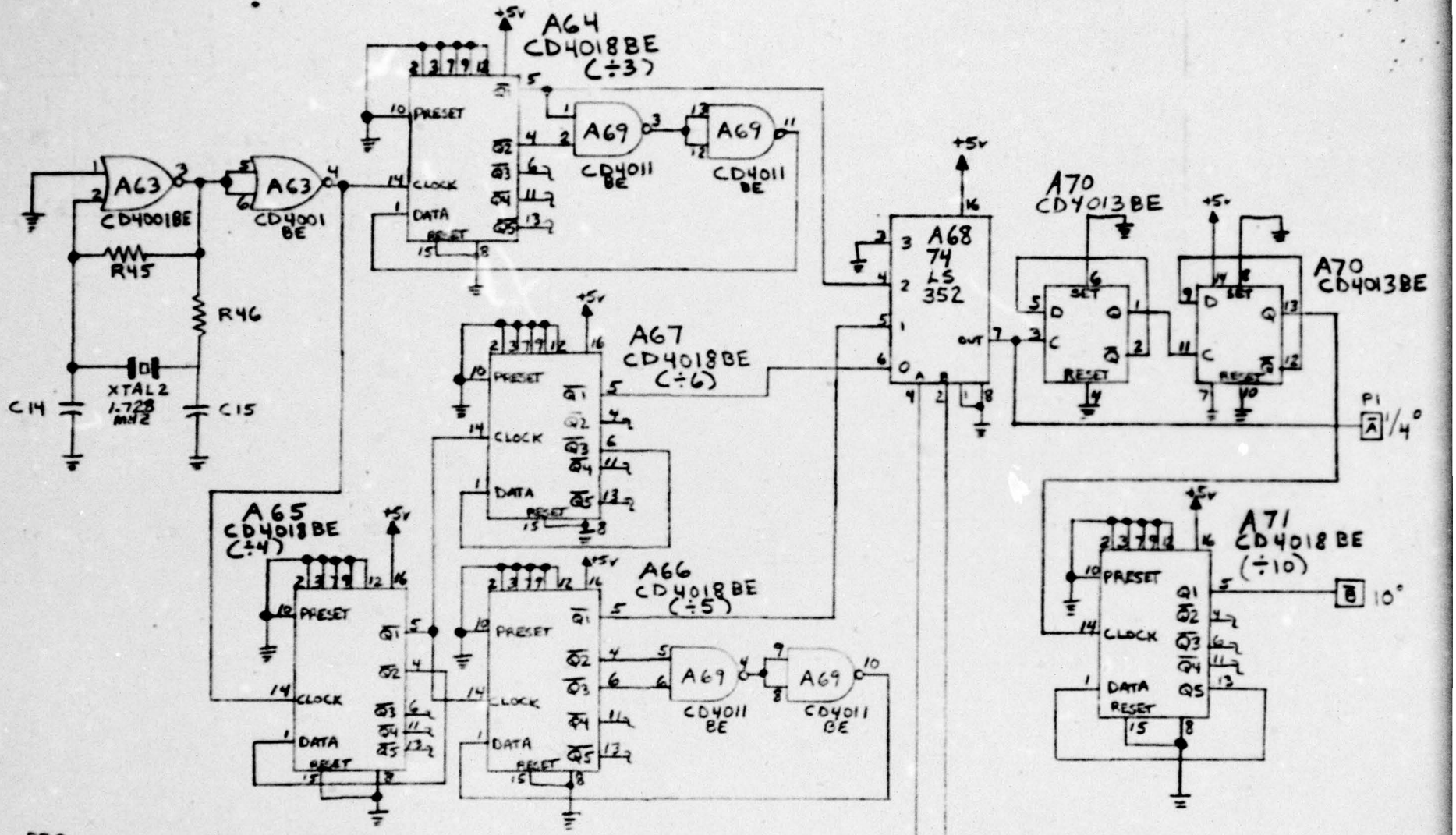


MPU BOARD SCHEMATIC
Sheet 3 of 6


RESET
+5V
IRQA
IRQB
A3L
MC6821
VCC
VSS
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
CA1
CA2
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
CB1
CB2
P1
PA 0
PA 1
PA 2
PA 3
PA 4
PA 5
PA 6
PA 7
PB 0
PB 1
PB 2
PB 3
PB 4
PB 5
PB 6
PB 7
* SEE NOTE
D0
D1
D2
D3
D4
D5
D6
D7
ADO
AD1
R/W BUFF
G OUT BUFF
RS0
RS1
R/W
E
CS1
CS2
CS0
A60
74LS11
COMM. FAIL INT
A3B
MC6821
AD5
AD6
RESET
IRQA
IRQB
PC 0
PC 1
PC 2
PC 3
PC 4
PC 5
PC 6
PC 7
MPU BOARD
Sheet 4 of 6
-32-
NOTE: NOT SHOWN ARE 10K PULL UP RESISTORS ON PB0 - PB7.



MPU BOARD
Sheet 5 of 6



MPU BOARD SCHEMATIC
Sheet 6 of 6

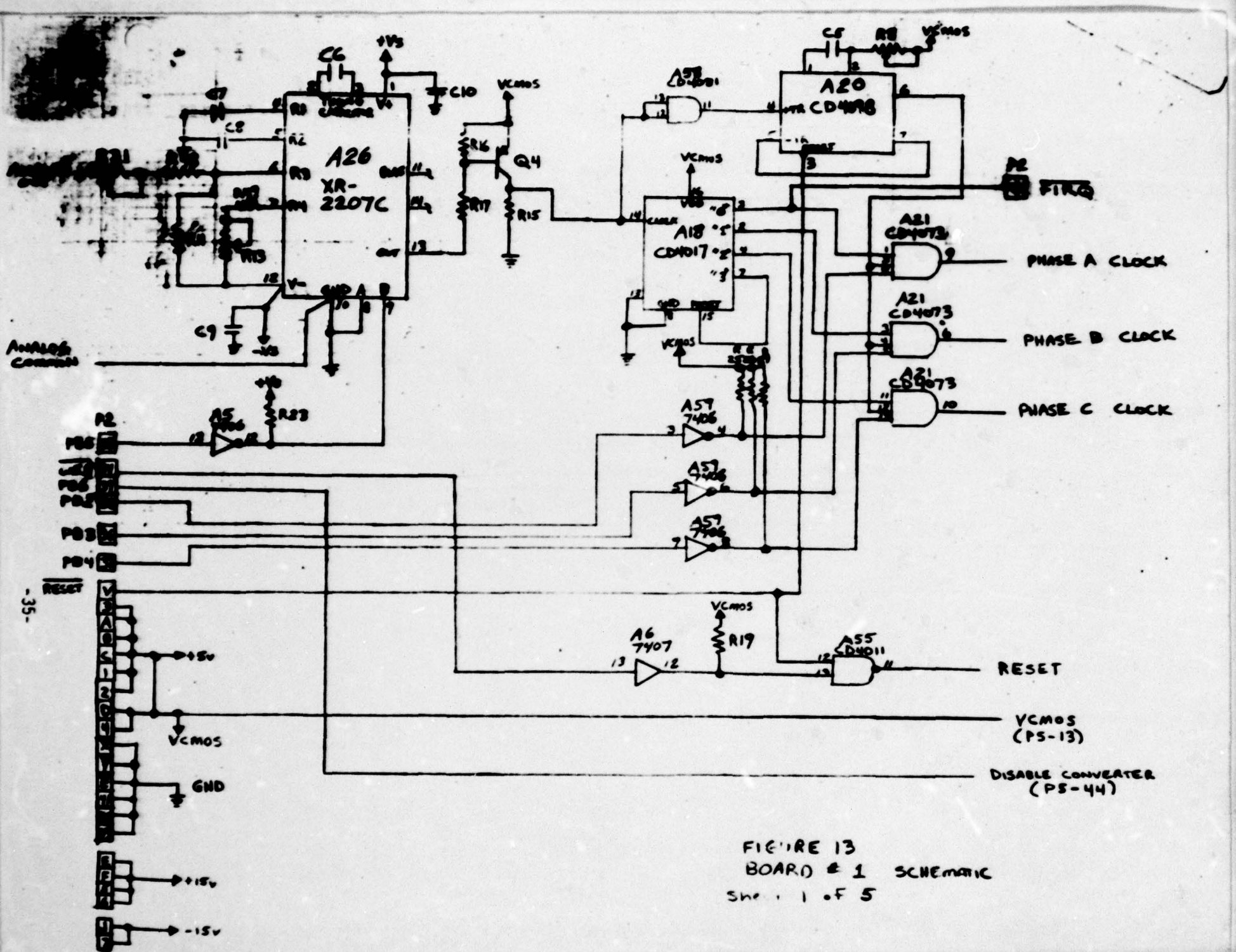
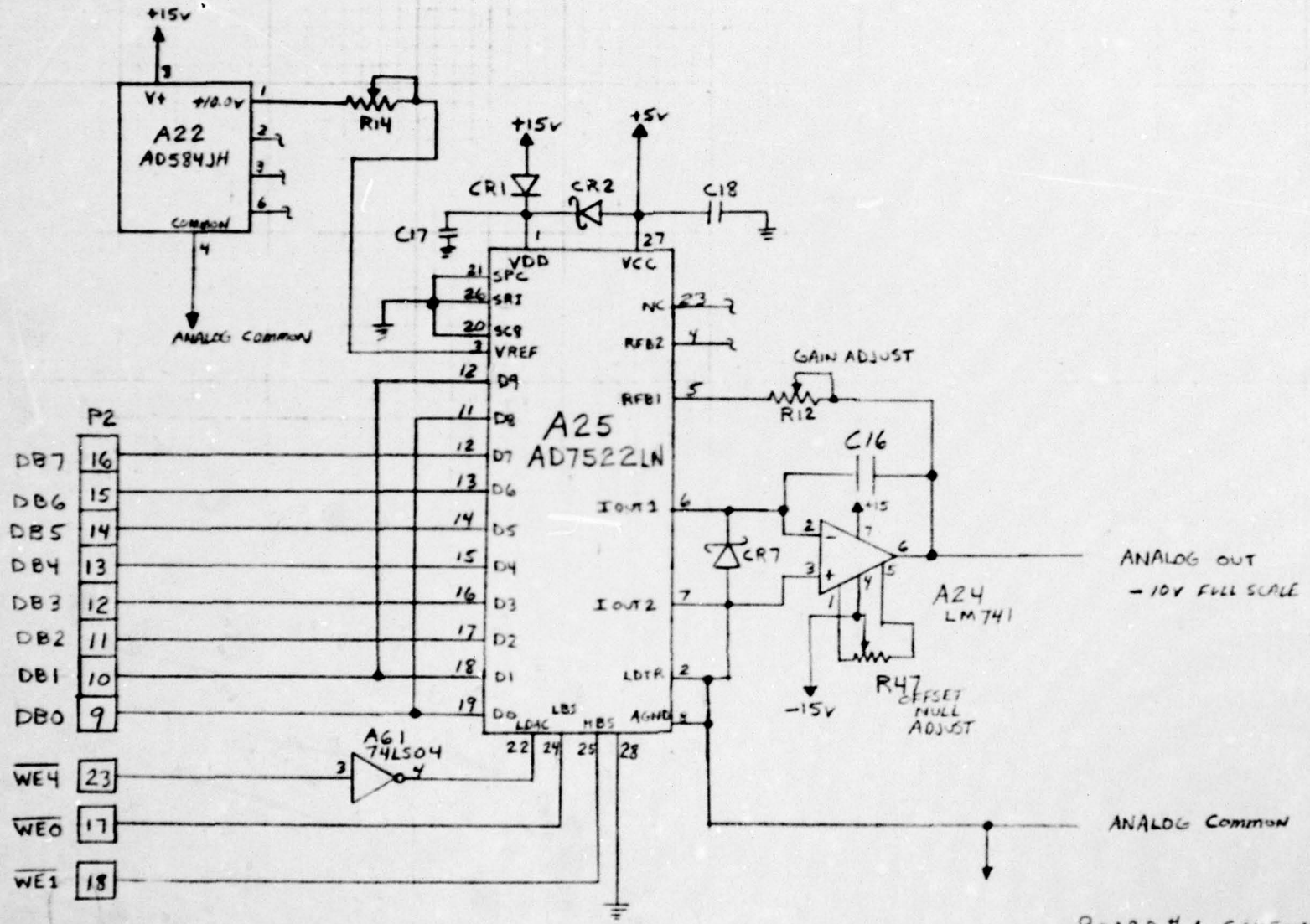
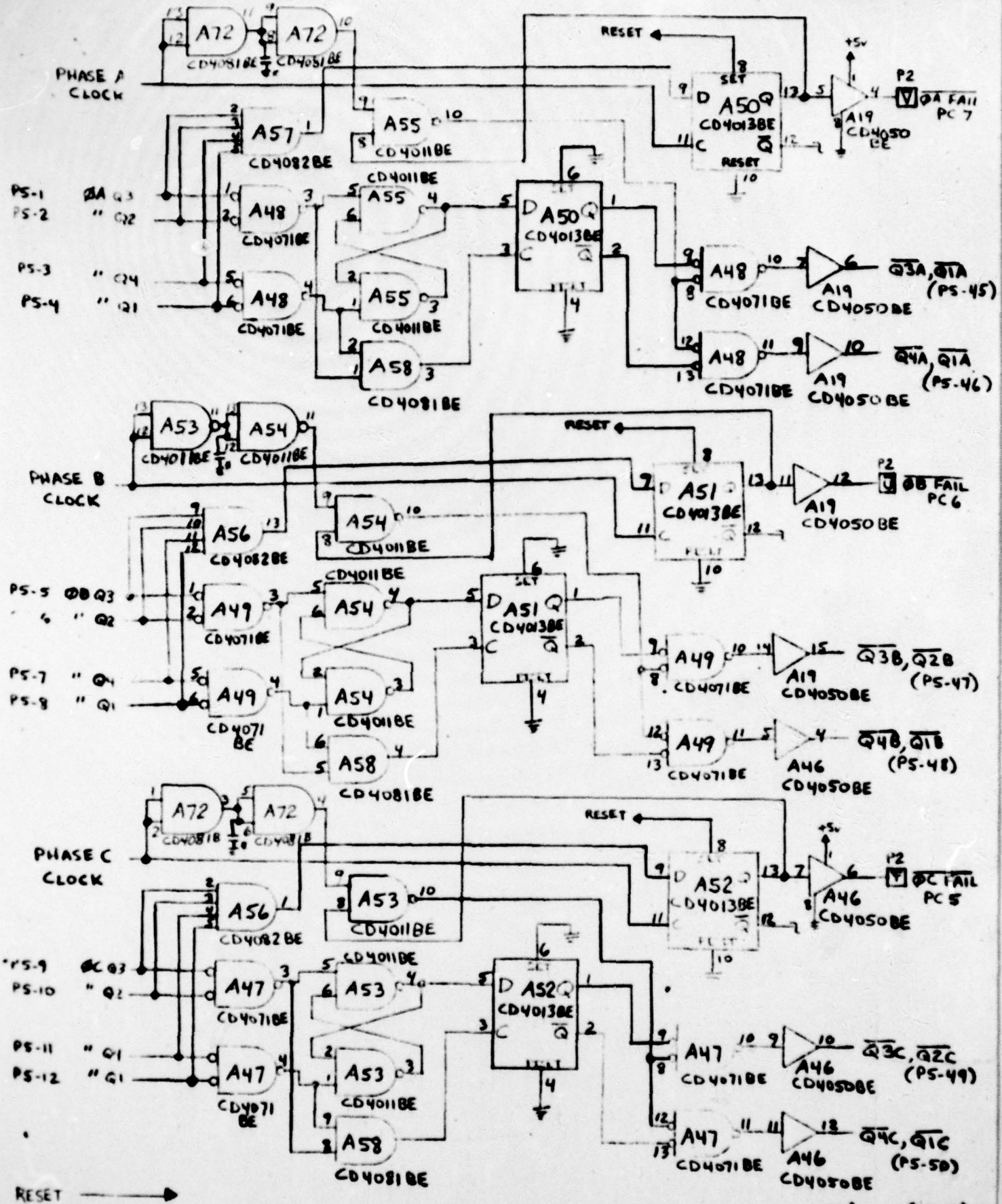


FIGURE 13
BOARD # 1 SCHEMATIC
SHT. 1 OF 5



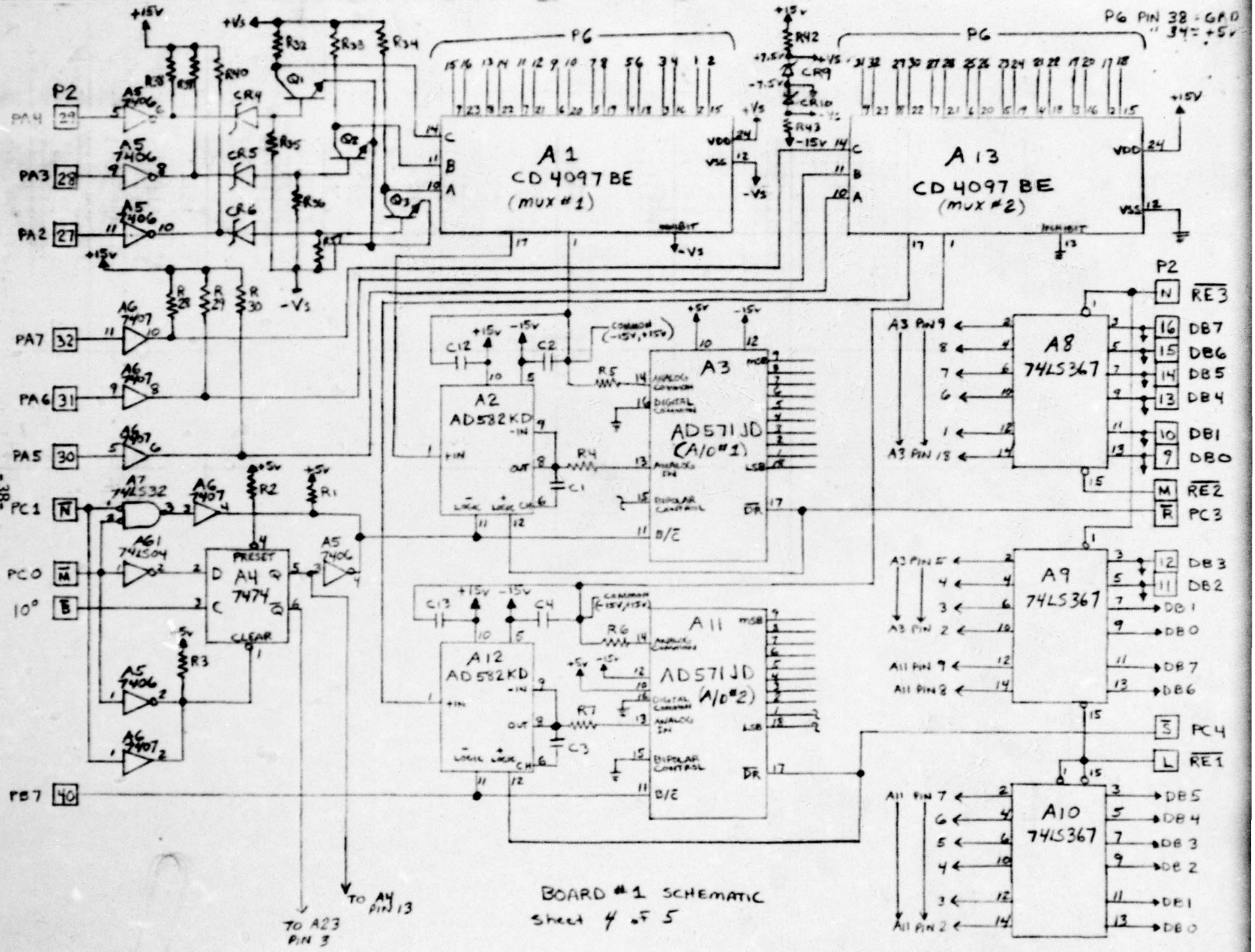
BOARD # 1 SCHEMATIC
Sheet 2 of 5

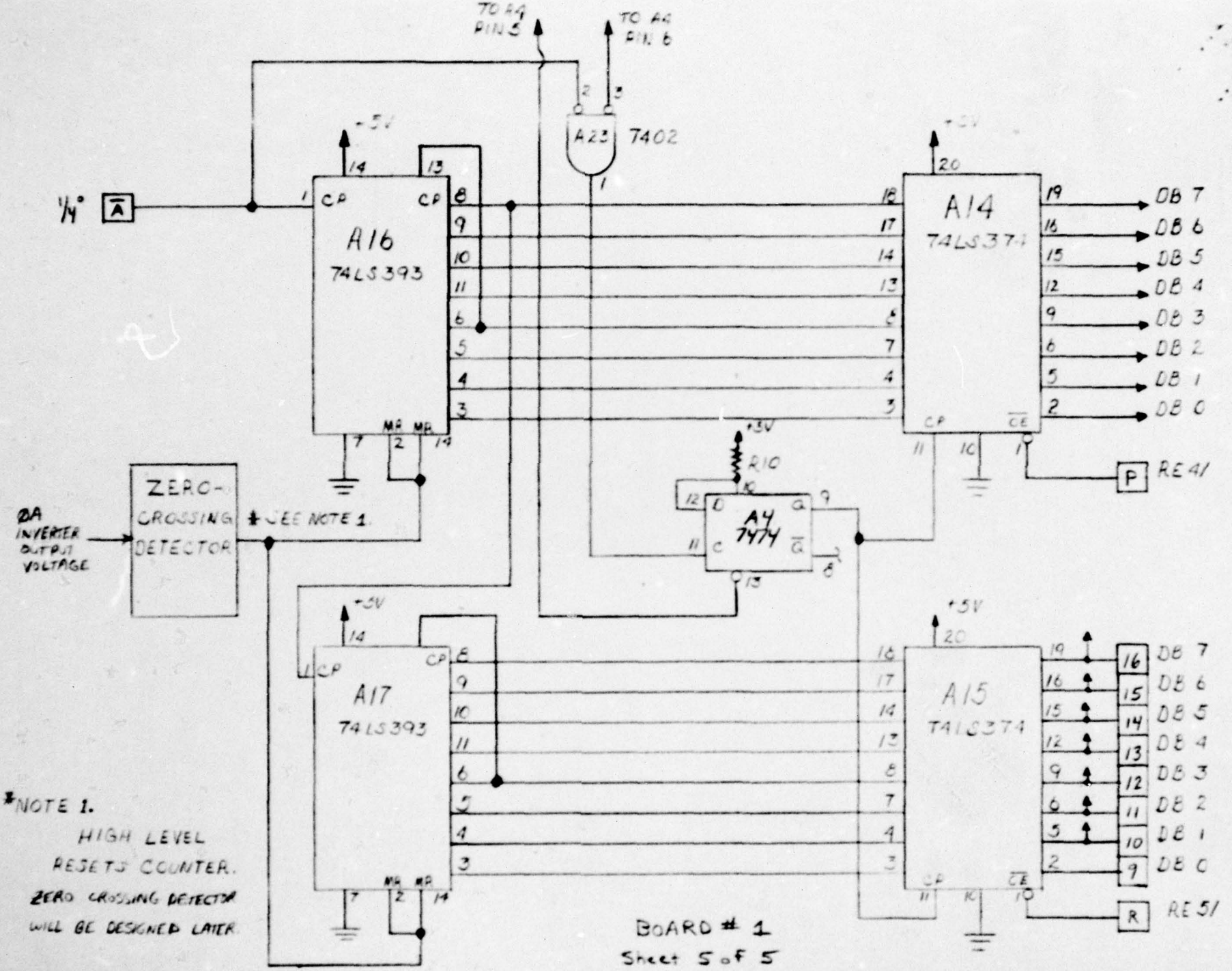


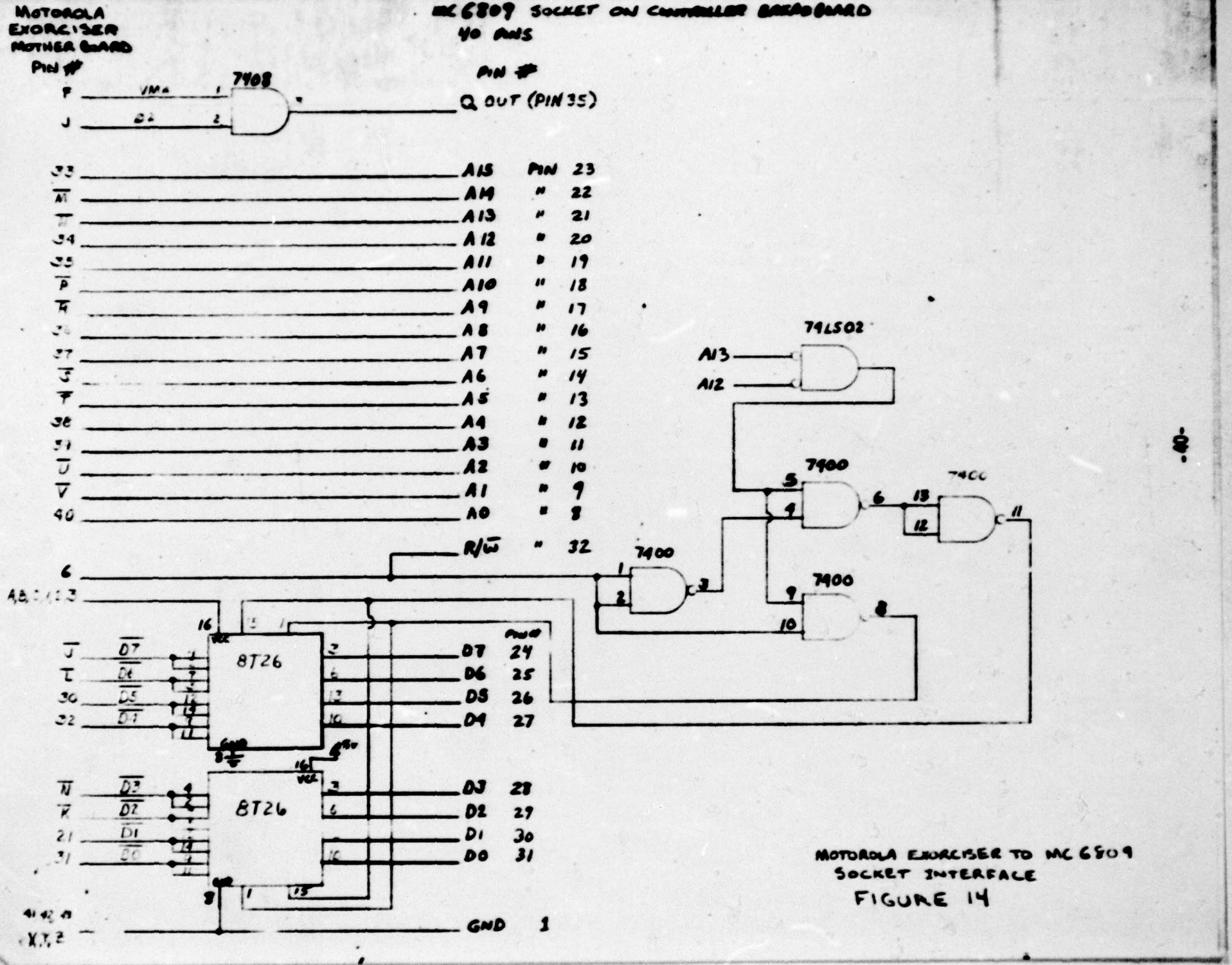
BOARD # 1 SCHEMATIC

Sheet 3 of 5

* These capacitors are not in parts list. They are optional. 470 pf.


P6 PIN 38 = GND
" 34 = +5V
A1
CD 4097 BE
(MUX #1)
A13
CD 4097 BE
(MUX #2)
A2
AD582KD
A3
AD571JD
(A/D #1)
A12
AD582KD
A11
AD571JD
(A/D #2)
A4
7474
A8
74LS367
A9
74LS367
A10
74LS367
P2
PA4
PA3
PA2
PA7
PA6
PA5
PC1
PC0
10°
PB7
RE3
DB7
DB6
DB5
DB4
DB1
DB0
RE2
PC3
DB3
DB2
PC4
RE1
TO A23 PIN 3
TO A4 PIN 13
BOARD #1 SCHEMATIC
Sheet 4 of 5

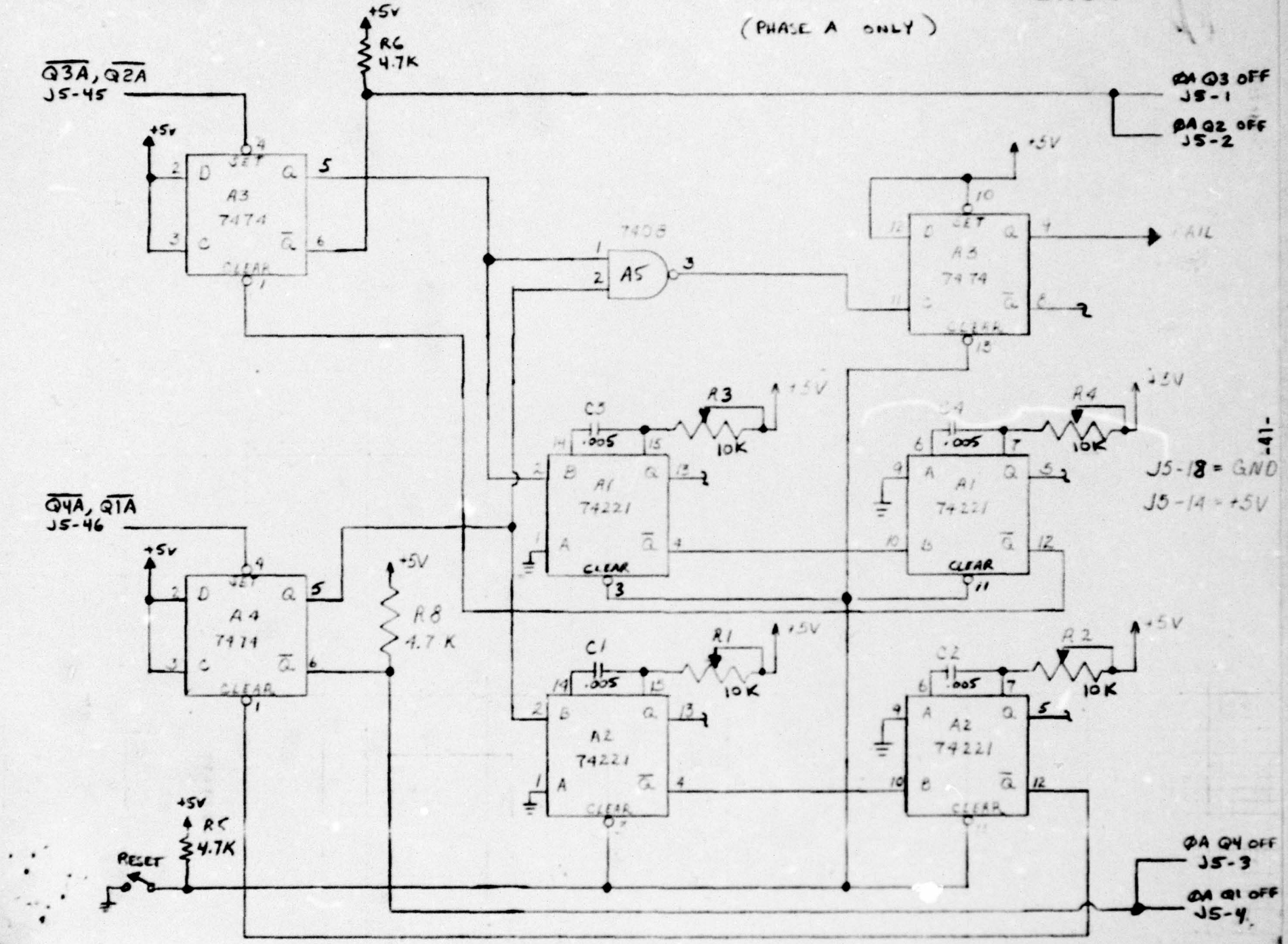

TO A4 PIN 5
TO A4 PIN 6
A23 7402
+5V
1/4°
A16 74LS393
CP
MR
A14 74LS374
DB 7
DB 6
DB 5
DB 4
DB 3
DB 2
DB 1
DB 0
CE
P
RE 41
R10
A4 7474
D
C
Q
ZERO-CROSSING DETECTOR
DA INVERTER OUTPUT VOLTAGE
* SEE NOTE 1.
A17 74LS393
A15 74LS374
R
RE 51
*NOTE 1.
HIGH LEVEL RESETS COUNTER.
ZERO CROSSING DETECTOR WILL BE DESIGNED LATER.
BOARD # 1
Sheet 5 of 5

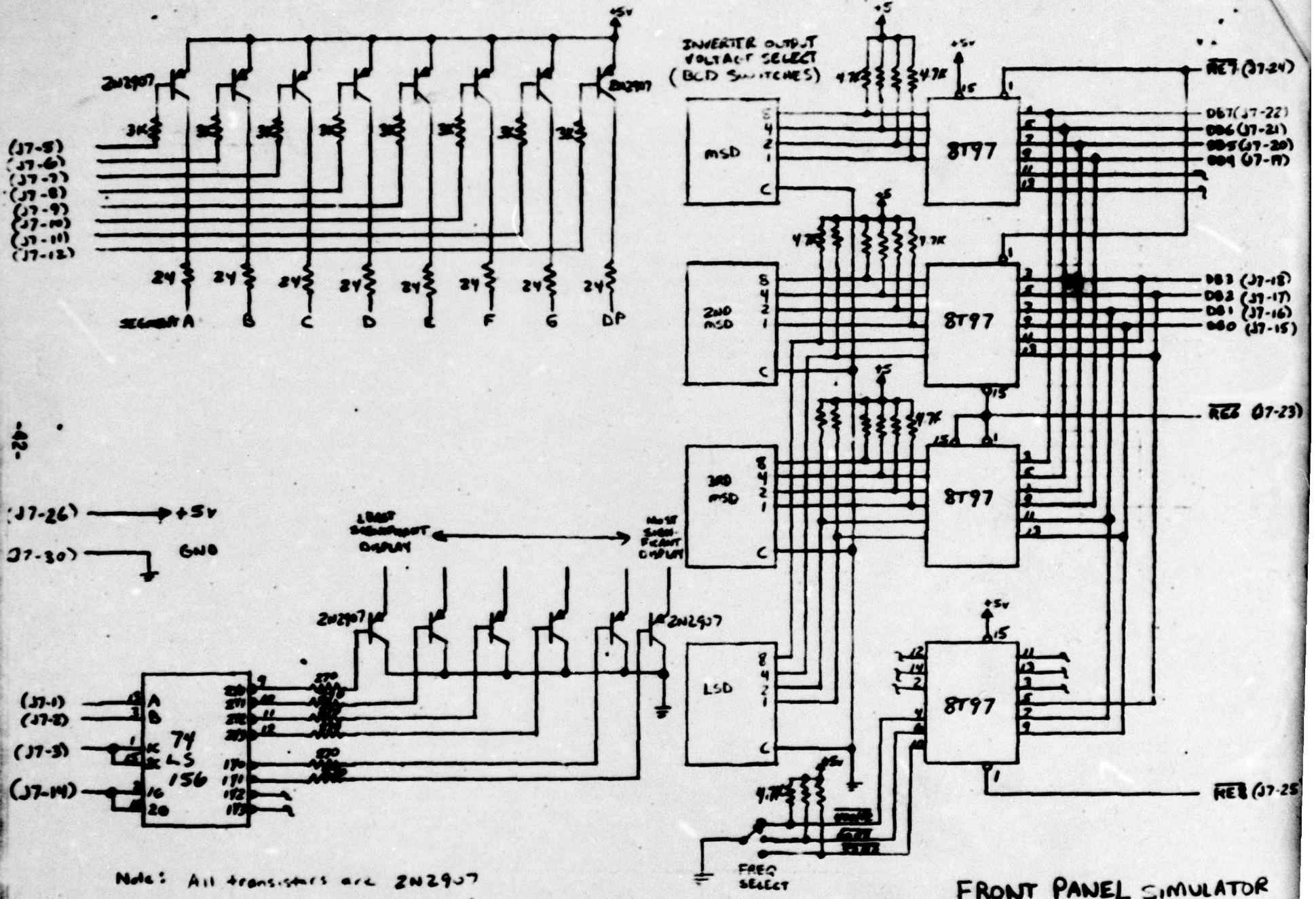


MOTOROLA EXORCISER TO MC6809 SOCKET INTERFACE

FIGURE 14

FIGURE 15
CONVERTER SCR SIMULATOR
(PHASE A ONLY)





Note: All transistors are 2N2907

FRONT PANEL SIMULATOR

FIGURE 16